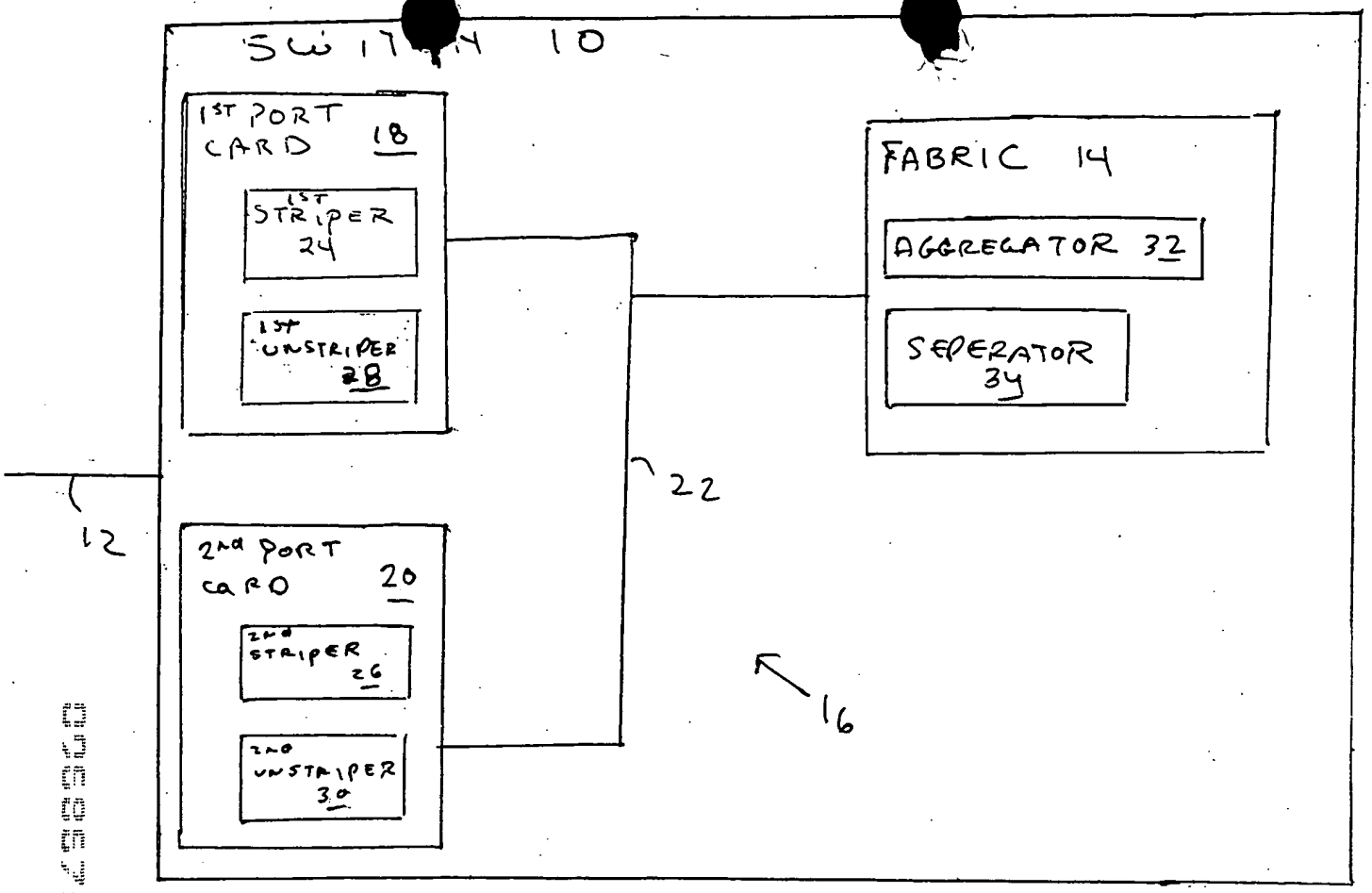
FIG 1


SWITCH 10
1ST PORT CARD 18
1ST STRIPER 24
1ST UNSTRIPER 28
FABRIC 14
AGGREGATOR 32
SEPERATOR 34
12
22
2ND PORT CARD 20
2ND STRIPER 26
2ND UNSTRIPER 30
16

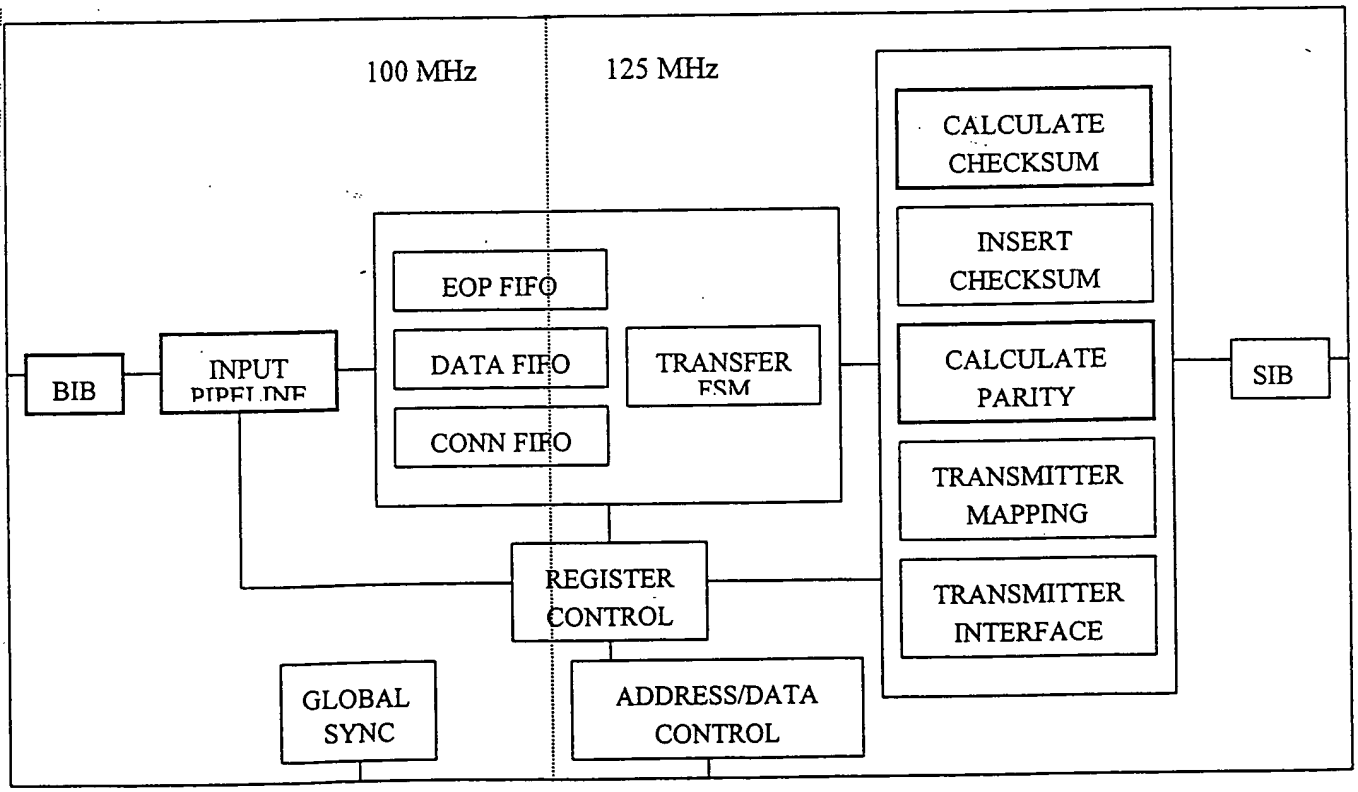

100 MHz
125 MHz
BIB
INPUT PIPELINE
EOP FIFO
DATA FIFO
CONN FIFO
TRANSFER FSM
REGISTER CONTROL
GLOBAL SYNC
ADDRESS/DATA CONTROL
CALCULATE CHECKSUM
INSERT CHECKSUM
CALCULATE PARITY
TRANSMITTER MAPPING
TRANSMITTER INTERFACE
SIB

FIG 2

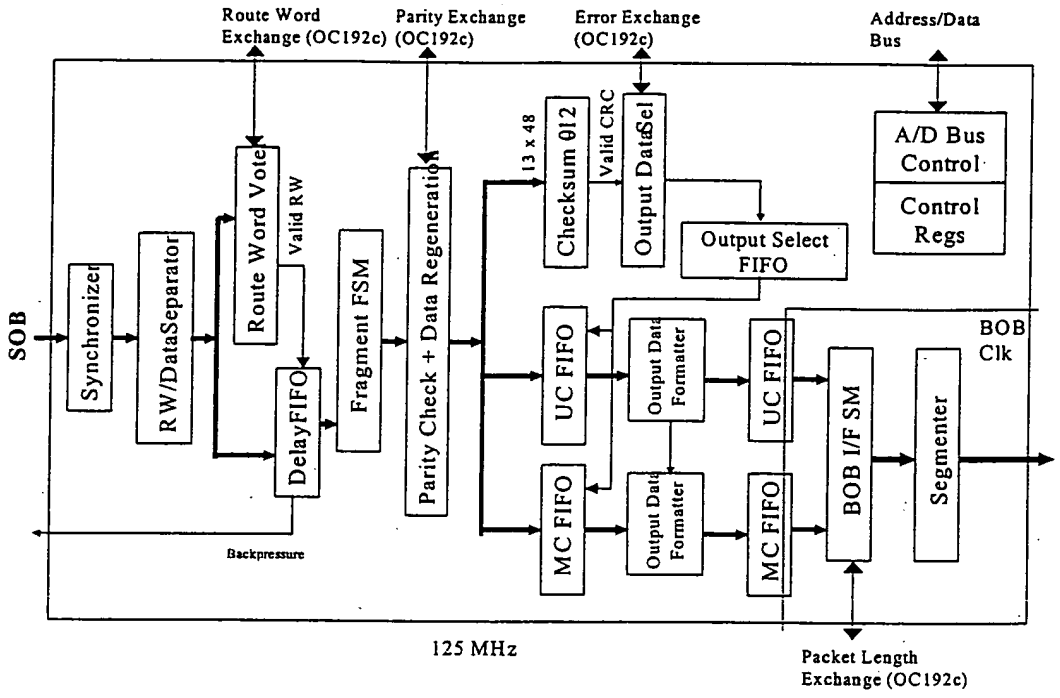

Route Word Exchange (OC192c)
Parity Exchange (OC192c)
Error Exchange (OC192c)
Address/Data Bus
SOB
Synchronizer
RW/DataSeparator
Route Word Vote
Valid RW
DelayFIFO
Fragment FSM
Parity Check + Data Regeneration
13 x 48
Checksum 012
Valid CRC
Output DataSel
Output Select FIFO
A/D Bus Control
Control Regs
UC FIFO
MC FIFO
Output Data Formatter
Output Data Formatter
UC FIFO
MC FIFO
BOB I/F SM
Segmenter
BOB Clk
Backpressure
125 MHz
Packet Length Exchange (OC192c)

FIG 3